REMARKS

In response to the Advisory Action mailed on August 10, 2007, an RCE with an accompany Amendment is being filed. Reconsideration is respectfully requested in view of the foregoing amendments and the comments set forth below.

By this Amendment, claims 1, 9-10, 21, 23 and 24 are amended and claims 27-29 are canceled. Accordingly, claims 1-7, 9-14, and 16-26 are pending in the present application.

Claims 1, 6, 10-11, 13, 17, 21 and 23-29 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2006/0206738 to Jeddeloh et al (hereinafter referred to as "Jeddeloh"). This rejection is traversed.

Jeddeloh is directed to a system and method for selective memory module power management where a power management controller 360 determines whether the memory module 300 is active or not based on signals from the activity monitor 350 and the temperature sensor 370. Paragraph [0028] of Jeddeloh discloses that temperature sensor 370 discerns an **average temperature** across an array of memory devices, or, alternatively sensor 370 could take the operating temperature of a sampling of memory devices 104 as being indicative of the operating temperature of each memory device 104. That is, Jeddeloh discloses power reduction of memory chips that are connected together on an average temperature of memory chips 104 attached to a memory module 300.

Paragraph [0029] of Jeddeloh discloses how the temperature sensor functions and states that it compares "the measured temperature to a predetermined threshold value". However, Jeddeloh discloses that the temperature may be an absolute value relative to an **ambient system temperature** or a differential measured from an operating temperature

reached by the **memory module 300** once it has become fully operational. Thus, Jeddeloh discloses measuring a temperature of the system or the memory module so that the power management controller could assume a reduced power state of the memory module through use of a self-refresh mode, or, the powering down of memory devices 104 that are completely idle, for example. This is not the claimed invention.

The claimed invention set forth in claims 1 and10 recites a chip and a device that measures the temperature of the chip, and means for regulating an operating voltage of the chip based on the temperature of the chip wherein the means for regulating an operating voltage changes the operating voltage of the chip to a minimum allowed voltage at its idle state, which is a low power state. That is, the claimed invention reduces the voltage, but does not turn it off, if the sensed or measured chip temperature is less than a predetermined state that represents an idle state of the chip. Independent claim 24 recites a method claims that measures temperature while the chip is on and reduces the operating voltage to an minimum allowed voltage power when the measured temperature of the chip drops below the idle state of the chip, which is a low power state. In each of the independent claims, the threshold temperature representing the idle state of the chip is determined based on speed characteristics of the chip at the threshold temperature, and the minimum allowed voltage and the threshold temperature maintain the speed characteristics of the chip, while providing significant reduction in power consumption of the chip.

At the very most, Jeddeloh discloses reducing the power. Nowhere does Jeddeloh disclose changing the operating voltage to the **minimum allowed voltage power** of an idle state, which is a low power state of the chip, as required by the claimed invention.

There is no disclosure in Jeddeloh of reducing voltage from a nominal amount to a minimal amount that will safely operate the system without compromise to performance. Jeddeloh simply discloses turning off the system. The turning off of the system in Jeddeloh is not the recited minimum allowed voltage power of an idle state where the idle state is a low power state of a chip. Jeddeloh also fails to disclose a threshold temperature as some predefined function of operational voltage and minimum allowed temperature (and still be operational) as required in each of the independent claims of the present application. Consequently, Jeddeloh cannot anticipate the claimed invention set forth in claims 1, 6, 10-11, 13, 17, 21 and 23-26 of the present application because it fails to disclose each and every recited feature of the claims. Withdrawal of this rejection is respectfully requested.

Claims 2-5, 9, 12 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh. This rejection is respectfully traversed.

Jeddeloh's system may not be functional under a reduced voltage that is a minimum allowed voltage because its system is directed to a different method of power reduction, as described above. The claimed invention reduces voltage in a system, but does not turn it off. The minimum voltage taught by Jeddeloh is to turn the voltage to zero, which is not a low power state of the chip as required in the claims. The present invention utilizes the fact that voltage and temperature impact the signal speed within the chip in an opposite way. Thus, when the internal temperature of a chip goes down (e.g., less chip activities, lower ambient temperature, better board thermal solution/heat removal, or the specific inherent properties of the Si chip), the temperature reduction allows the device to reduce voltage safely without causing functional failure of the chip.

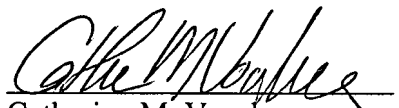
That is, the reduced internal signal within the Si chip maintains required speed and does not cause timing violations (compromise the performance of the chip). Consequently, the threshold temperature could be a constant number or a function of operational voltage, minimum allowed device temperature (and still be operational) and inherent speed characteristics of the chip. See paragraphs [0014]-[0015] and [0018] of the present application.

In view of the above, it is submitted that Jeddeloh does not disclose a system where reducing the operating voltage to a minimum allowed voltage value would work. Consequently, Jeddeloh cannot render obvious the claimed inventions and withdrawal of the rejection under §103(a) is respectfully requested.

For the above stated reasons, it is submitted that all of the claims are allowable over the prior art of record and are in condition for allowance. Therefore, it is respectfully submitted that this application be passed to issuance with claims 1-7, 9-14, and 16-26.

Should the Examiner believe that a conference would advance the prosecution of this application, he is encouraged to telephone the undersigned counsel to arrange such a conference.

Respectfully submitted,



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Catherine M. Voorhees
Registration No. 33,074
VENABLE LLP
P.O. Box 34385
Washington, DC 20043-9998
Telephone: (202) 962-4800
Telefax: (202) 962-8300

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